CLAIMS

What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. An image sensor readout circuit, comprising:

a column line for receiving a plurality of analog pixel and analog reset signals; and

a binning circuit coupled to said column line, wherein said binning circuit combines a predetermined plurality of analog pixel signals and outputs them on a first output line, and combines a predetermined plurality of analog reset signals and outputs them on a second output line.

2. The readout circuit of claim 1, wherein said binning circuit comprises:

a first sample circuit, said first sample circuit storing the plurality of analog pixel signals; and

a second sample circuit, said second sample circuit storing the plurality of analog reset signals.

3. The readout circuit of claim 2, wherein the first sample circuit comprises:

a first plurality of sample switches; and

a first plurality of capacitive elements, wherein each of said first plurality of sample switches are coupled to a respective one of said first plurality of capacitive elements, said first plurality of capacitive elements being further coupled to the first output line.

4. The readout circuit of claim 3, wherein the second sample circuit comprises:

a second plurality of sample switches; and

a second plurality of capacitive elements, wherein each of said second plurality of sample switches are coupled to a respective one of said second plurality of capacitive elements, said second plurality of capacitive elements being further coupled to the second output line.

5. The readout circuit of claim 4, wherein the first and second plurality of sample switches and capacitive elements comprise an even number of sample switches and capacitive elements.

6. A binning circuit for an image sensor, comprising:

a column line for receiving analog pixel and analog reset signals of an active pixel sensor;

a first sample circuit coupled to said column line, said first sample circuit storing a plurality of analog pixel signals;

a second sample circuit coupled to said column line, said second sample circuit storing a plurality of analog reset signals;

a first switch coupled to the first sample circuit and to a first output line, said first switch being controlled to combine the plurality of analog pixel signals and output the combined pixel signals on the first output line; and

a second switch, coupled to the second sample circuit and to a second output line, said second switch being controlled to combine the plurality of analog reset signals and output the combined reset signal on the second output line.

7. The binning circuit of claim 6, wherein the first sample circuit comprises:

a first plurality of sample switches; and

a first plurality of capacitive elements, wherein each of said first plurality of sample switches are coupled to a respective one of said first plurality of capacitive elements, said first plurality of capacitive elements being further coupled to the first output line.

8. The binning circuit of claim 7, wherein the second sample circuit comprises:

a second plurality of sample switches; and a second plurality of capacitive elements, wherein each of said second plurality of sample switches are coupled to a respective one of said second plurality of capacitive elements, said second plurality of capacitive elements being further coupled to the second output line.

9. The binning circuit of claim 8, wherein the first and second plurality of sample switches and capacitive elements comprise an even number of sample switches and capacitive elements.

10. A method of binning the output of an active image sensor, comprising:

sampling analog output signals from the sensor according to a first predetermined sequence;

sampling analog reset signals from the sensor according to a second predetermined sequence;

combining and outputting all sampled analog output signals on a first line; and

combining and outputting all sampled analog reset signals on a second line.

11. The method according to claim 10, wherein said step of sampling said analog output signals comprises storing each analog output signal in a respective capacitive element according to the first predetermined sequence.

12. The method according to claim 10, wherein said step of sampling said analog reset signals comprises storing each analog reset signal in a respective capacitive element according to the second predetermined sequence.

13. The method according to claim 10, wherein the first and second predetermined sequences are determined by a less-than-full pixel resolution condition.

14. The method according to claim 13, wherein the first and second predetermined sequences further comprise interpolating different row output and reset signals from a column readout circuit in said active image sensor.

15. The method according to claim 14, wherein the predetermined sequence further comprises sampling identical colors from different rows from a column readout circuit in said active image sensor.

16. The method according to claim 13, wherein the first and second predetermined sequences further comprise interpolating different column readout circuits in said active image sensor.

17. The method according to claim 10, wherein the first and second predetermined sequence is determined by a Bayer pattern.

18. The method of claim 10, wherein at least one of said first and second acts of combining comprises:

subtracting said sampled signals.

19. The method of claim 18 further comprising:

calculating a color separation value of sampled signals of said sensor.

20. A charge-domain readout circuit comprising:

a plurality of column readout circuits each of which sample and store multiple pixel signals and reset signal values of an active pixel sensor, wherein each column readout circuit is associated with a respective column of sensors in the active pixel sensor;

a first bus for receiving pixel signal values stored by a selected one of the column readout circuits; and

a second bus for receiving the reset signal values stored by a selected one of the column readout circuits

21. The circuit of claim 20, wherein each column readout circuit includes a plurality of sample and hold circuits.

22. The circuit of claim 21, wherein each sample and hold circuit comprises:

a plurality of charge storage elements; and

a plurality of first switches, each of said plurality of switches being coupled to a respective one of said plurality of charge storage elements, wherein said plurality of switches can be selectively enabled to sample a signal from a sensor in the array to be stored by the charge storage element.

23. The circuit of claim 22, wherein each column readout circuit comprises a plurality of second switches which can be selectively enabled to hold one side of the charge storage elements at a reference voltage when a corresponding one of the first switches is enabled to sample a value from a sensor.

24. The circuit of claim 22, wherein each column readout circuit includes a switch that can selectively enabled to short together one side of each charge storing element.

25. The circuit of claim 20, further comprising column switches coupled between each of the column

readout circuits, wherein the column switches can be selectively enabled to couple together the stored pixel signal and reset signal values present on the column of sensors in an active pixel sensor.

26. A method of reading out values from active pixel sensors in an array of sensors, the method comprising:

selecting multiple rows of sensors whose values are to be read out;

storing correlated double sampled values for a plurality of sensors in the selected rows, wherein the values for each sensor are stored by a respective readout circuit associated with a column in the array in which the sensor is located;

combining the stored signals; and

sensing the stored values associated with the plurality of sensors in the selected rows using an operational amplifier-based charge sensing circuit that is common to the readout circuits.

27. The method of claim 26 wherein the act of storing correlated double sampled values includes sampling and storing a signal value of a sensor and sampling and storing a reset value of the sensor.

28. The method of claim 27 including setting a reference voltage on first sides of respective capacitive elements and subsequently coupling the signal and reset values to second sides of the respective capacitive elements.

29. The method of claim 28 wherein setting a reference voltage includes providing the reference voltage from the common operational amplifier-based charge sensing circuit.

30. The method of claim 29 wherein sensing the stored values includes using a crowbar switch to force charge stored in each respective readout circuit onto feedback capacitive elements in the operational amplifier-based charge sensing circuit.

31. A processing system, comprising:

a processing circuit;

an imaging circuit coupled to said processing circuit, said imaging circuit having a charge-domain readout circuit, said readout circuit comprising:

a plurality of column readout circuits each of which can sample and store multiple pixel signal and reset values of an active pixel sensor, wherein each column readout circuit is

associated with a respective column of sensors in an active pixel sensor;

a first bus for receiving pixel signal values stored by a selected one of the column readout circuits; and

a second bus for receiving the pixel reset values stored by a selected one of the column readout circuits.

32. The processing system of claim 31, wherein each column readout circuit includes a plurality of sample and hold circuits.

33. The processing system of claim 32, wherein each sample and hold circuit comprises:

a plurality of charge storage elements; and

a plurality of first switches, each of said plurality of switches being coupled to a respective one of said plurality of charge storage elements, wherein said plurality of switches can be selectively enabled to sample a signal from a sensor in the array to be stored by the charge storage element

34. The processing system of claim 33, wherein each column readout circuit comprises a plurality of second switches which can be selectively enabled to hold one side of the charge storage elements at a reference voltage when a

corresponding one of the first switches is enabled to sample a value from a sensor.

35. The processing system of claim 34, wherein each column readout circuit includes a switch which selectively can be enabled to short together one side of each charge storing element.

36. The processing system of claim 35, further comprising column switches coupled between each of the column readout circuits, wherein the column switches can be selectively enabled to couple together the stored pixel signal and reset values present on the column of sensors in an active pixel sensor.